DESIGN FOR TEST OF ANALOG MODULE SYSTEMS

ABSTRACT

An apparatus for testing an integrated circuit that includes analog nodes is disclosed. In one aspect, an integrated circuit comprises testing circuitry and core logic circuitry. A memory in the testing circuitry stores data identifying analog nodes in the core logic circuitry and tolerance values associated with the analog nodes. A condition checker compares actual test values with the associated tolerance values. A main control unit controls the testing circuitry and synchronizes testing of the core logic circuitry. In another aspect, the testing circuitry includes a host computer interface useful for communicating with a host computer. A data memory in the testing circuitry is used for storing diagnostic data. The contents of the data memory may then be uploaded to a host computer. Test stimuli may be transmitted to the integrated circuit from a location outside the integrated circuit to perform testing.